REMARKS

Claims 1-38 are pending in this application. Claims 1, 23, 27, 28, 29, and 31-37 have been amended in several particulars in accordance with current Office policy, to further define Applicants' disclosed invention relative to cited prior art and to assist the Examiner to expedite compact prosecution of the instant application.

Again, the Examiner has requested submission of a clean copy of the marked-up specification filed on November 27, 2001 because the handwritten changes were too small and difficult to read, and a statement that the Substitute Specification contains no new matter. However, this request is subjective, unreasonable and unwarranted under 37 C.F.R. § and MPEP. The handwritten changes made to the original specification on November 27, 2001 are not too small and, certainly not difficult to read as alleged. Moreover, Applicants have already certified that the Substitute Specification as filed on November 27, 2001 is accurate and contains no new matter. Such a certification is sufficient under the MPEP and, there is no need, nor is there any requirement that the original specification be re-submitted with handwritten changes to the satisfaction of the Examiner. As a result, the original specification will **not** be marked up again. Unless there is an express prohibition under 37 C.F.R. § or MPEP, which Applicants are not aware, the Examiner request should be withdrawn. Nevertheless, if the Examiner insists submission of such a revised specification, authority from 37 C.F.R. or MPEP is respectfully requested.

Claims 1, 9, 11, 14-17, 21-23, 24, 26, 27, 29-31 and 36-38 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Yamaguchi et al., U.S. Patent

No. 5,627,557 in view of newly cited art, Booth Jr. et al., U.S. Patent No. 6,742,915 for reasons stated on pages 3-9 of the non-final Office Action (Paper No. 6). Specifically, in support of Applicants' base claim 1, the Examiner asserts that Yamaguchi '557 discloses all features except for "a refreshing operation means for performing a preset refreshing operation to signal charge stored in the memory capacitor." However, the Examiner cites column 16, lines 46-55 of Booth '915, as a secondary reference, for allegedly disclosing:

> "a display panel (100) including an array (106) of liquid crystal display pixel cells (125). Each of the pixel cells (125) may be part of a display element (120), a circuit that stores a change that indicates an intensity of a pixel that is formed by the pixel cell (see column 3, lines 32-49). An update circuit (130) includes a storage unit (124) that stores the terminal voltage across the associated pixel cell (125) after each update. That is the storage unit (123) includes a capacitor (142) that has a much larger capacitance than the capacitor of the pixel cell (125). The display panel may use the storage units (124) to regularly refresh the pixel cells (125) automatically without receiving new image data. Booth also teaches that each storage unit (124) may include a transistor that is activated to couple the capacitor (142) to the pixel cell (125) to refresh the terminal voltage across the pixel cell (125 (see column 5, lines 6-42)."

This disclosure is cited to support an assertion that "it would have been obvious ... to allow the usage of the update circuit including the capacitor for refreshing the voltages in the pixel cell arrangement which is taught by Booth" to arrive at Applicants' base claim 1.

However, the Examiner's assessment of what Yamaguchi '557 discloses is incorrect. Likewise, the Examiner's citation of Booth '915, as a secondary reference, is also misplaced. As a result, this rejection is respectfully traversed for the following reasons.

First of all, base claims 1, 28, 29, 31, 36 and 37 have been amended to expressly define the "display data" as –digital display data– to further distinguish over the Examiner's newly proposed combination of Yamaguchi, U.S. Patent No. 5,627,557 and Booth Jr. et al., U.S. Patent No. 6,642,915. This is because Booth '915 discloses a display panel, as shown in FIG. 5 and FIG. 6, in which **analog indications** of a terminal voltage of a pixel cell are stored and subsequently used to refresh the terminal voltages. See Summary section of Booth '915. In other words, an analog signal voltage (as opposed to digital display data as per Applicants' base claims 1, 27, 28, 29, 31, 36 and 37) from the D/A converter 103 is stored or written in the storage unit 124, in advance in the liquid crystal pixel 125. The increment part voltage having written from the outside is then added in order to generate a new (analog) signal voltage. If the increment part voltage is not added, then the original analog signal voltage having written in the liquid crystal pixel 125 becomes the new signal voltage. As described by Booth '915, the purpose of the storage unit 124 is to mitigate the lost amount (the vanishing amount) of the analog signal voltage. The "refresh" operation intended by Booth '915 is **not** to recover the lost signal, but to mitigate the vanishing (the lost) of the analog signal voltage. As a result, Booth '915 provides no mechanism to recover data or reliably rewrite data, and the analog signal voltage will be lost in time due to a leak current.

Therefore, as amended, base claims 1, 28, 29, 31, 36 and 37 are believed to be distinguishable over Yamaguchi, U.S. Patent No. 5,627,557 and Booth Jr. et al., U.S. Patent No. 6,642,915.

To the extent that the rejection may still be applicable, Applicants respectfully submit that Yamaguchi, U.S. Patent No. 5,627,557 and Booth Jr. et al., U.S. Patent

No. 6,642,915, whether taken individually or in combination, disclose or suggest Applicants' base claims 1, 27, 28, 29, 31, 36 and 37.

For example, Applicants' base claim 1 defines an image display apparatus comprising:

> a plurality of display pixels arranged in a matrix to provide image display, each of said display pixels having a pixel electrode and a pixel switch connected to said pixel electrode in series;
> a plurality of memory elements for storing digital display data;
> image signal generating means for outputting a given image signal based on said digital display data;
> a group of signal lines for connecting said image signal generating means to a group of pixel switches; and
> display image selection means for writing said image signal in a given display pixel through said group of signal lines and a group of pixel switches,
> wherein each basic unit of said memory element comprises a memory switch; a memory capacitor connected to said memory switch; an amplifier field-effect transistor (FET) of which a gate is connected to said memory capacitor; and refreshing operation means for performing a preset refreshing operation to rewrite a signal charge stored in said memory capacitor using said amplifier FET.

As defined in Applicants' base claim 1, for example, the image display apparatus comprises (1) a plurality of memory elements for storing [digital] display data; (2) image signal generating means for outputting a given image signal based on [digital] display data; and (3) means for writing image signal in a given (predetermined) display pixel. Each basic unit of the memory element comprises the memory switch, the memory capacitor connected to the memory switch, the amplifier field-effect transistor (FET) and refreshing operation means for performing a preset refreshing operation to rewrite a signal charge (digital display data) stored in the memory capacitor **using the amplifier FET**. Such an amplifier FET is used as the low electric power consumption of the sense amplifier during the data reading-out from the memory cell, as described on page 3, lines 11-21, page 9, lines 5-18, and

FIG. 2 of Applicants' specification. In addition, the "refresh" operation as described, for example, on page 17, lines 7-10 of Applicants' specification, refers to the rewriting of previous [digital] display data stored in the memory cell.

In contrast to Applicant's base claim 1, Yamaguchi '557 discloses a display apparatus, as shown in FIG. 14, in which a pixel is provided with a holding capacitance as a capacitance element and a pixel capacitance as a display element, as shown in FIG. 1. The purpose of Yamaguchi '557 is to remove the effect of a large leak current in the pixel capacitance, as described on column 1, lines 31-35, and column 2, lines 24-31. In order to achieve this purpose, Yamaguchi '557 utilizes a transistor provided in a memory cell as a buffer to drive the pixel capacitance having the large leak current.

According to Yamaguchi '557, on the cited column 16, lines 46-55 and FIG. 16, the "refresh" is used in the context of "elimination (cancellation, clear, deletion) of the previous data, which has already read out from the image element capacitor. Such a refresh operation is **not**, and can**not** possibly be interpreted to read on Applicants' claimed "refreshing operation means [part of the memory element] for performing a preset refreshing operation to rewrite a signal charge stored in said memory capacitor using said amplifier FET" as expressly defined, for example, in Applicants' base claim 1.

Booth '915, as a secondary reference, does **not** remedy the noted deficiencies of Yamaguchi '557 in order to arrive at Applicants' base claim 1. This is because Booth '915 only discloses a display panel, as shown in FIG. 5 and FIG. 6, in which **analog indications** of a terminal voltage of a pixel cell are stored and

subsequently used to refresh the terminal voltages, as discussed previously. As a result, the analog signal voltage will be lost in time due to a leak current.

Nevertheless, the Examiner cites column 3, lines 32-49 and column 5, lines 6-42 of Booth '915 for allegedly disclosing "storage units (124) to regularly refresh the pixel cells (125) automatically without receiving new image data"" in order to support an assertion that "it would have been obvious ... to allow ... usage of a refreshing signal" to arrive at Applicants' base claims 1, 28-29, 31 and 35-38.

This citation is misplaced, however. The cited column 5, lines 6-42 of Booth '915 refer to the updating of the analog signal voltage across the pixel cell. This is used to mitigate the lost amount of the analog signal voltage, and **not** to recover lost signal. Certainly, this is contrary to Applicants' claimed "refresh operation" in which such a "refresh operation" indicates (means, shows) the "rewriting of the previous data" stored in the memory cell.

As a result, there is **no** disclosure anywhere from the Examiner's proposed combination of Yamaguchi '557 and Booth '915 of Applicants' claimed "memory element comprises a memory switch; a memory capacitor connected to said memory switch; an amplifier field-effect transistor (FET) of which a gate is connected to said memory capacitor; and refreshing operation means for performing a preset refreshing operation to rewrite a signal charge stored in said memory capacitor using said amplifier FET" as expressly defined in Applicants' base claim 1.

Again, in order to establish a *prima facie* case of obviousness under 35 U.S.C. §103, the Examiner must show that the prior art reference (or references when combined) must teach or suggest all the claim limitations, and that there must be some suggestion or motivation, either in the references themselves or in the

knowledge generally available to one of ordinary skilled in the art, to modify the reference or to combine reference teachings, provided with a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and **not** based on Applicants' disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP 2143. In other words, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USQP 494, 496 (CCPA 1970). Moreover, "obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination." ACS Hospital System, Inc v. Montefiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). The Examiner must point to something in the prior art that suggests in some way a modification of a particular reference or a combination of references in order to arrive at Applicants' claimed invention. Absent such a showing, the Examiner has improperly used Applicants' disclosure as an instruction book on how to reconstruct to the prior art to arrive at Applicants' claimed invention. Furthermore, any deficiencies in the cited references cannot be remedied with conclusions about what is "basic knowledge" or "common knowledge". See In re Lee, 61 USPQ 2d 1430 (Fed. Cir. 2002).

In the present situation, both Yamaguchi '557 and Booth '915 fail to disclose and suggest key features of Applicants' base claims 1, 28-29, 31 and 35-38.

Therefore, Applicants respectfully request that the rejection of Applicants' base claims 1, 28-29, 31 and 35-38 and their dependent claims be withdrawn.

With respect to Applicants' base claims 29, 31, 36, 37 and 38, Applicants respectfully traverse the rejection for the same reasons presented against the rejection of Applicants' base claim 1.

Dependent claims 2-8, 10, 18-20 and 24 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Yamaguchi et al., U.S. Patent No. 5,627,557 in view of Booth Jr. et al., U.S. Patent No. 6,642,915 as applied to claim 1 above, and further in view of Parks, U.S. Patent No. 5,471,225 for reasons stated on pages 9-11 of the Office Action (Paper No. 6). Since the correctness of this rejection is predicated upon the correctness of the rejection of Applicants' base claim 1, Applicants respectfully request that the rejection of dependent claims 2-8, 10, 18-20 and 24 be withdrawn for the same reasons discussed.

Lastly, claim 28 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Yamaguchi et al., U.S. Patent No. 5,627,557 in view of Yamazaki et al., U.S. Patent No. 6,335,716 and Parks, U.S. Patent No. 5,471,225 for reasons stated on pages 11-12 of the Office Action (Paper No. 6). Specifically, in support of this rejection, the Examiner further cites Parks '225 for allegedly disclosing the "image signal generating means having a reference voltage generating circuit using a poly-Si thin film resistor". However, this citation is also misplaced. Accordingly, Applicants respectfully traverse the rejection for reasons discussed herein below.

Base claim 28, as amended, defines an image display apparatus comprising:

> a plurality of display pixels arranged in a matrix in order to provide image display, each display pixel having a pixel electrode and a pixel switch connected to said pixel electrode in series;

> image signal generating means for outputting an image signal based on digital display data;
>
> a group of signal lines for connecting said image signal generating means to a group of pixel switches; and
>
> display image selection means for writing said image signal in a given display pixel through said group of signal lines and said group of pixel switches, at least said plurality of display pixels, said group of signal lines and said image signal generating means being formed on a single transparent substrate,
>
> wherein said image signal generating means has a reference voltage generating circuit using a boron-doped polycrystalline Si (poly-Si) thin-film resistor as a gray scale voltage generating resistor.

As expressly defined in Applicants' base claim 28, the "image signal generating means has a reference voltage generating circuit using the boron-doped polycrystalline Si (Poly-Si) thin film resistor as a gray scale voltage generating resistor." Such a feature is described as follows.

> "However, since boron (B) does not occur such segregation, the resistance values are stable, and in addition the sheet resistance value is an appropriate valve of several k." See page 12, lines 11-13 of Applicants' specification.

> "Therefore, the poly-Si thin film doped with boron (B) is not suitable for the gray scale voltage generating resistor 53 because the electric power consumption is small, and the area is not large, and the values of generated gray scale power source voltage are stable." See page 12, lines 11-15 of Applicants' specification.

> "Table 2 shows measured values of dispersion in sheet resistance of a boron (B) doped poly-Si thin film and a phosphorus (P) thin film.
>
> Since the dispersion in sheet resistance of the phosphorus (P) thin film is above 4 times as large as that of the boron (B) doped poly-Si thin film." See page 12, lines 15-18 of Applicants' specification.

Nowhere in Yamaguchi '557, Yamazaki '716 or Parks '225, and the Examiner has **not** addressed, is there any disclosure of Applicants' claimed "reference voltage generating circuit using the boron-doped polycrystalline Si (poly-Si) thin film resistor as a gray scale voltage generating resistor" as defined in Applicants' base claim 28.

Since Yamaguchi '557, Yamazaki '716 or Parks '225 fail to disclose and suggest key features of Applicants' base claim 28, Applicants respectfully request that the rejection of Applicants' base claim 28 be withdrawn.

In view of the foregoing amendments, arguments and remarks, all claims are deemed to be allowable and this application is believed to be in condition to be passed to issue. Should any questions remain unresolved, the Examiner is requested to telephone Applicants' attorney at the Washington DC area office at (703) 312-6600.

INTERVIEW:

In the interest of expediting prosecution of the present application, Applicants respectfully request that an Examiner interview be scheduled and conducted. In accordance with such interview request, Applicants respectfully request that the Examiner, after review of the present Amendment, contact the undersigned local Washington, D.C. area attorney at the local Washington, D.C. telephone number (703) 312-6600 for scheduling an Examiner interview, or alternatively, refrain from issuing a further action in the above-identified application as the undersigned attorneys will be telephoning the Examiner shortly after the filing date of this Amendment in order to schedule an Examiner interview. Applicants thank the Examiner in advance for such considerations. In the event that this Amendment, in and of itself, is sufficient to place the application in condition for allowance, no Examiner interview may be necessary.

To the extent necessary, Applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage of fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, No. 01-2135 (Application No. 503.40029X00), and please credit any excess fees to said deposit account.

Respectfully submitted,

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